AMENDMENT TO THE SPECIFICATION

Please amend the specification as follows:

Please replace the paragraph appearing on page 9, line 27 (the last paragraph on page 9) to page 10, line 7 (the first partial paragraph on page 10) as follows:

Even with the use of a higher Radix and modified Booth recoding the number and size of partial products that are generated when multiplying numbers having a greater number of bits can become large. Addition of these partial products can become complex and can consume a large area on the integrated circuit, particularly if the bits can be combined in only small groups. In one embodiment of the present invention, these partial products are added by a shift ~~an~~and recode method, which significantly reduces complexity and speeds computation time.

Please replace the paragraph appearing on page 18, lines 3-12 with the following amended paragraph:

At step 201, word 220 is divided into groups of adjacent bits to form a first level of multiple-bit groups 226. In this example, each of the groups 226 includes two or three bits. The number of bits in each group can be set based on convenience ~~and~~or on a maximum number of transistors that can be connected in series with one another in the technology in which the integrated circuit will be fabricated. Each group 226 can include any number of bits in alternative embodiments of the present invention.

Please replace the two paragraphs appearing on page 20, lines 3-24 with the following amended paragraphs:

FIG. 10 is a schematic diagram illustrating a 2-bit shift circuit 250 for shifting each 2-bit group 226 shown in row 201 of FIG. 9. Circuit 250 includes a logic OR gate 251 and a logic AND gate 252. Inputs A0 and A1 represent the two inputs bits, and ~~Y0~~B0 and ~~Y1~~B1 represent the two output bits. A similar 2-bit shift circuit is used to shift each 2-bit group 226.

FIG. 11 is a schematic diagram illustrating a 3-bit shift circuit 260 for shifting the bits in each 3-bit group 226 in row 201 of FIG. 9. Circuit 260 includes logic OR gates 261 and 262 and logic AND gates 263, 264 and 265. Inputs ~~A0~~A2, ~~A1~~A3, and ~~A2~~A4 represent the least significant, middle, and most significant bit positions in a corresponding 3-bit group 226. Outputs ~~Y0~~B0, ~~Y1~~B1 and ~~Y2~~B2 represent the least significant, middle and most significant bit positions, respectively, in the respective modified 3-bit group 228. In one embodiment, the packing circuit includes one 3-bit shift circuit 260 for each 3-bit group 226. Again, any combination of logic can be used in alternative embodiments of the present invention.

Please replace Table 2 appearing on page 23, lines 2-15 with the following amended table:

Table 2

BITS 9876543210	ENCODING	ENCODED BINARY WORD
0000000000	ZERO = !D0	0000
0000000001	ONE = !D1&D0	0001
0000000011	TWO = !D2&D1	0010
0000000111	THREE = !D3&D2	0011
0000001111	FOUR = !D4&D3	0100
0000011111	FIVE = !D5&D4	0101
0000111111	SIX = !D6&D5	0110
0001111111	SEVEN = !D7&D6	0111

0011111111	EIGHT = !D8&D7	1000
0111111111	NINE = !D9&D8	1001
1111111111	TEN = ~~!D9~~D9	1010

Please replace the two paragraphs appearing on page 25, lines 3-26 with the following amended paragraphs:

As mentioned above, the circuit can be modified to accommodate a multiplier-accumulate (MAC) operation. For ~~an~~a MAC operation, an accumulation result is kept in the format of a carry-sum pair. This pair of binary numbers is fed back to the multiplier as if they were part of the original M/2 partial products, similar to rows 101 and 102 shown in FIG. 7. Using this mechanism, the multiplier result will be the multiplication of A and B plus the accumulator values. This mechanism incurs minimal cost to perform ~~an~~a MAC operation, and a final binary addition is carried out to sum the carry-sum pair at the next stage. Therefore, the throughput is a single cycle MAC operation.

With the ~~above-embodiments~~above embodiments, partial products can be added together faster while using less hardware. Existing methods combine partial products using 3-to-2 full bit-adders. The above embodiments allow more adder reduction options, such as 3-to-2, 7-to-3, 15-to-4, 31-to-5, etc., and thus can add many partial products together more quickly. The difference becomes more pronounced as the lengths of the multipliers and multiplicands increase and thus involve more partial products.

AMENDMENT TO THE DRAWINGS

Please amend FIG. 4 as shown in red in the enclosed, marked-up drawing.